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A Low-Cost FPGA-based Embedded Fingerprint Verification and Matching System

Maitane Barrenechea

Jon Altuna Miguel San Miguel

Signal Theory and Communications Group Department of Electronics University of Mondragon



- Software Architecture
- Hardware Architecture
- Conclusions

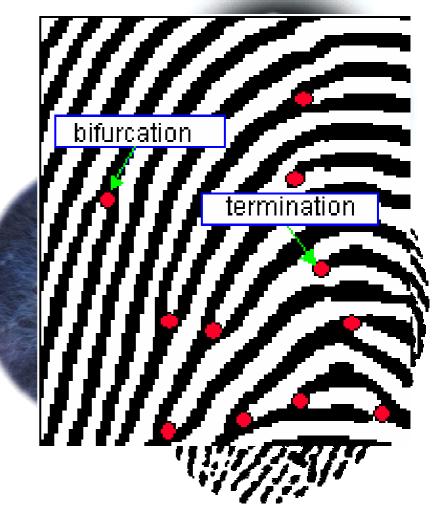


- Software Architecture
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- Uses some **unique** behavioural or physiological characteristics to identify a person.
- Behavioural characteristics:
 - Signature
 - Gait
 - Typing pattern
- Physiological characteristics:
 - Fingerprints
 - Facial Patterns
 - Hand Measurements
 - Eye Retinas



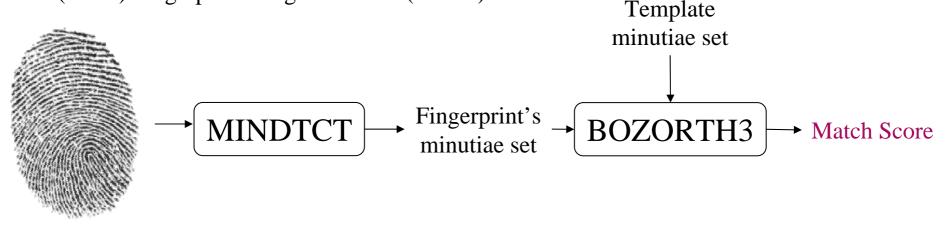


System Overview



Software

Based on the packages from the National Institute of Standard and Technology's (NIST) Fingerprint Image Software (NFIS2).



- Hardware
 - Spartan3 family FPGA
 - Leon2 32-bit Sparc Processor
 - Floating Point Unit (FPU)
 - Hardware co-processor
 - Fujitsu MBF200 fingerprint sensor

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Software Architecture

Hardware Architecture

Conclusions

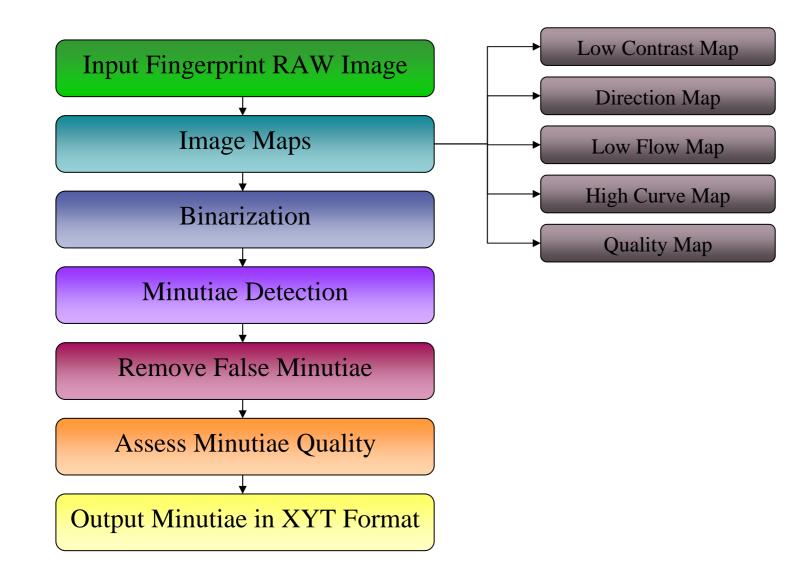


• Custom version of the MINDTCT and BOZORTH3 packages (NIST2).

- •Only those modules required for XYT formatted minutiae output set generation have been used.
- Input fingerprint image format modified \rightarrow RAW
- Used fingerprint images fulfil the conditions set for an optimum performance
 - **5**00 dpi
 - 256 greyscale
- Bare-C Cross-Compiler
- GRMON debug monitor

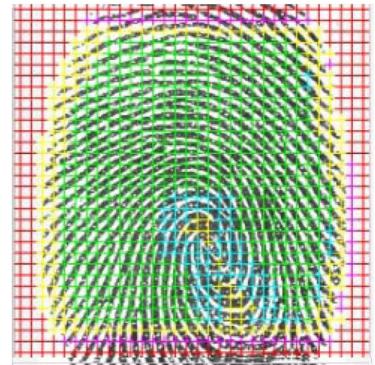
Minutiae Extraction Algorithm







- Low Contrast Map: Marks low contrast areas in the image.
- **Direction Map**: Represents the main ridge flow direction.
- Low Flow Map: Identifies image areas with a weak ridge structure.
- **High Curve Map**: Flags high curvature areas in the image.
- Quality Map: Assigns a quality level to each block in the image.
 - Poor quality
 - 🗕 Fair quality
 - Good quality
 - Very good quality
 - Excellent quality





Binarization & Minutiae Extraction

Binarization

• A pixel is assigned a binary value based on the ridge flow direction associated with the block the pixel is within.

Minutiae Extraction

Identify certain pixel patterns
Ridge Ending
Bifurcation

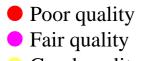






Remove False MinutiaeAssess Minutia Quality

- Two factors are combined to produce a quality measure:
 - Quality MapPixel Intensity Statistics



- Good quality
- Very good quality
- Excellent quality

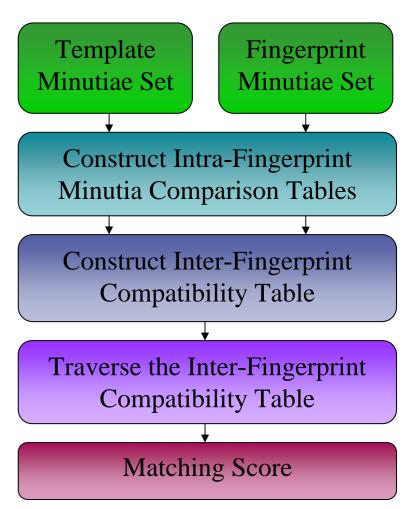




Bozorth3

- Rotation and translation invariant
- Matching Score > 40

Finger Match





Software Architecture

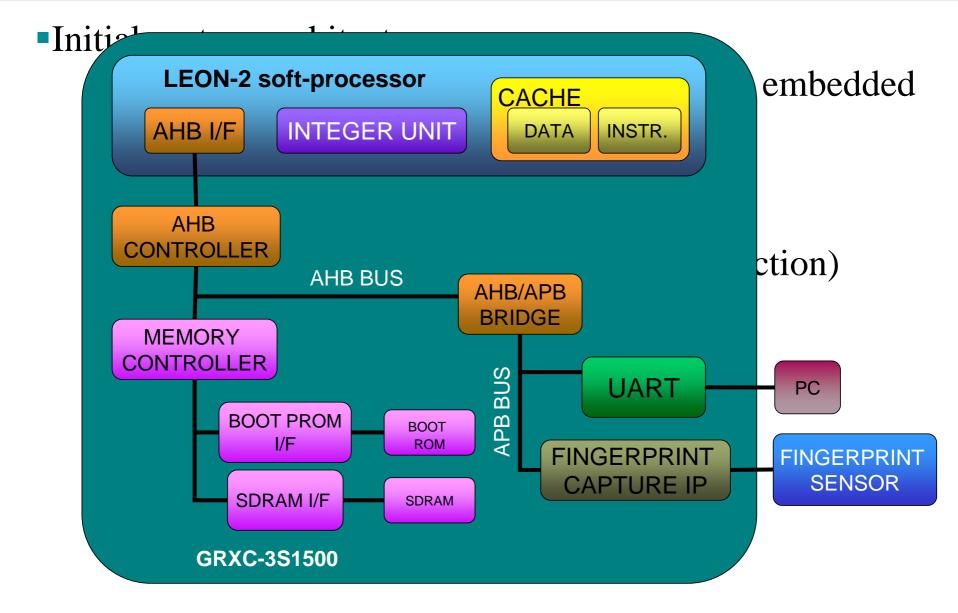
Hardware Architecture

Conclusions



Initial System Architecture







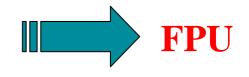
Initial System Architecture

- •Why Leon2?
 - High configurability
 - •VHDL code availability (under LGPL license).
 - High performance
 - Best performance per clock cycle
 - High usability
 - *Tkconfig* graphical configuration tool



- The execution of the algorithm is successful in terms of the matching results.
- Yet the execution time is excessive.
 - MINDTCT occupies 75% of the computation time.
- MINDTCT acceleration:
 - Mainly floating-point operations
 - Leon2 is a fixed-point processor
- Leon2 compatible FPUs:
 - LTH
 - Meiko
 - GRFPU

IEEE-754 compliant





- FPU insertion is Great increase in the amount of logic
 - Reduce clock frequency
 - Reduce cache sizes
- Three different system configurations under test
 - 31 MHz and 8KB cache memory.
 - 37 MHz and 8KB cache memory.
 - 40 MHz and 4KB cache memory.





Stanford benchmark

Measures the execution time in ms for ten small programs.

	Α	В	С	D	
Perm	34	50	33	34	A: 50 MHz / 8KB cache /No FPU. B: 31 MHz / 8KB cache / FPU. C: 37 MHz / 8KB cache / FPU. D: 40 MHz / 4KB cache / FPU.
Towers	50	83	67	50	
Queens	33	50	33	33	
Intmm	166	133	100	116	
Mm	1000	84	50	67	→ 91.6% - 95% execution time reduction
Puzzle	317	450	350	350	
Quick	50	50	33	33	
Bubble	50	50	50	50	
Tree	233	334	266	250	
FFT	1067	83	67	50	→ 92.22% - 95.3% execution time reduction

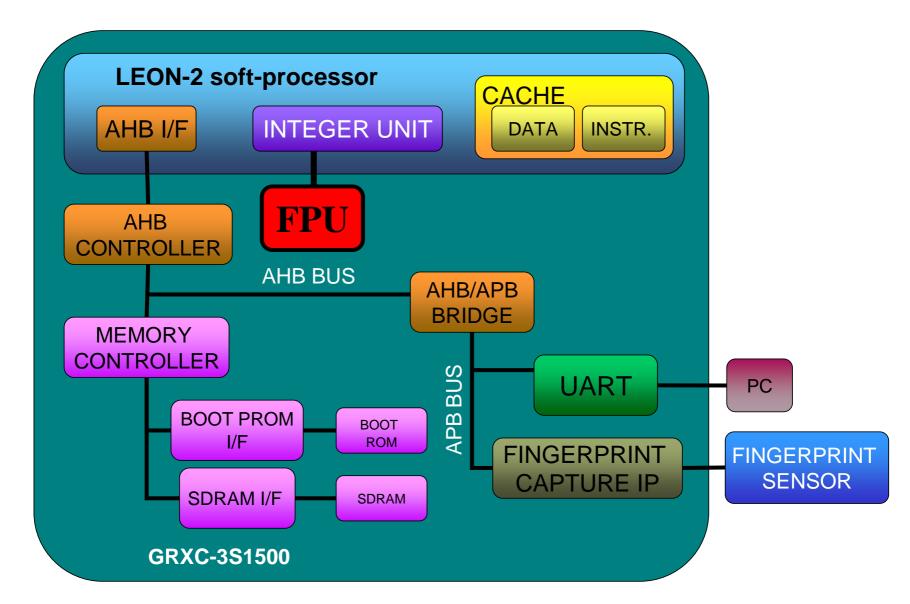
Paranoia benchmark

• Test the compliance with the IEEE-754 floating-point standard

HW Architecture

Introducing the GRFPU in the design





HW Architecture





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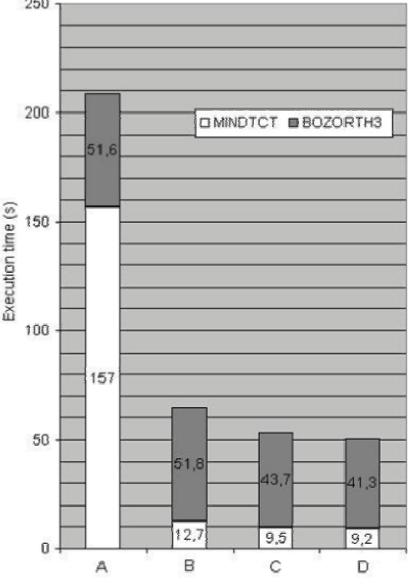
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 94.14% execution time reduction (40MHz / 4KB cache).

Program completion delay is yet excessive.

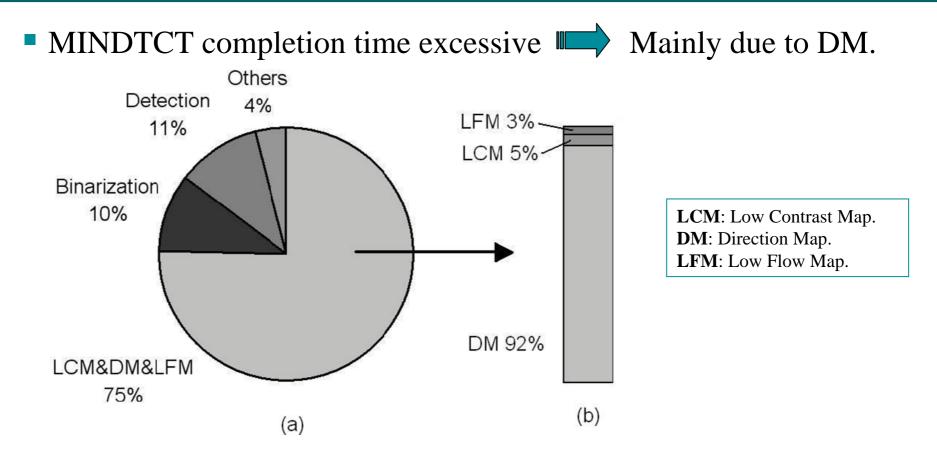
A: 50 MHz / 8KB cache /No FPU / No HW Co-processor.
B: 31 MHz / 8KB cache / FPU / No HW Co-processor.
C: 37 MHz / 8KB cache / FPU / No HW Co-processor.
D: 40 MHz / 4KB cache / FPU / No HW Co-processor.





HW speed enhancement

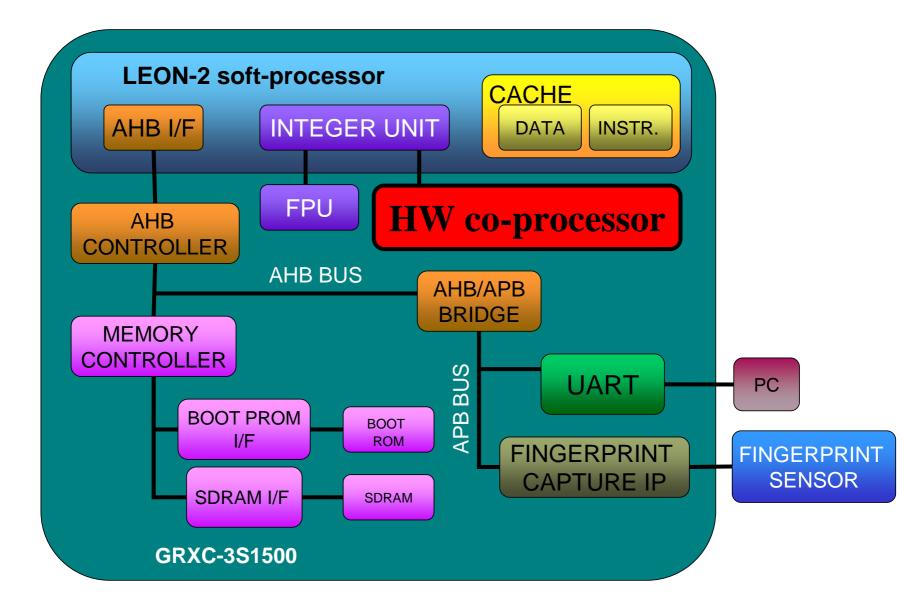




• HW accelerator speeds up this process

HW speed enhancement





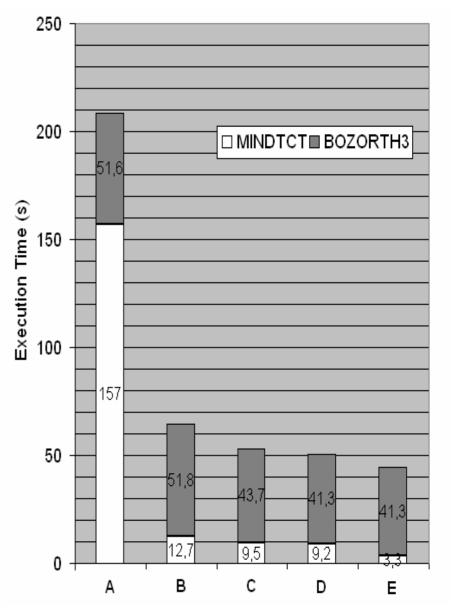
HW Architecture

HW speed enhancement



97.89% execution time reduction is estimated (40MHz / 4KB cache).

A: 50 MHz / 8KB cache /No FPU / No HW Co-processor.
B: 31 MHz / 8KB cache / FPU / No HW Co-processor.
C: 37 MHz / 8KB cache / FPU / No HW Co-processor.
D: 40 MHz / 4KB cache / FPU / No HW Co-processor.
E: 40 MHz / 4KB cache / FPU / HW Co-processor.





Software Architecture

Hardware Architecture

Conclusions



 Implementation of a fingerprint minutiae extraction and matching algorithm

- Spartan3 based low-cost system
- Embedded Leon2 soft-processor.
- Minutiae extraction process has been accelerated in a 94.14%.
- HW co-processor is estimated to speed-up the MINDTCT algorithm up to a 97.89%.
- Commercial systems use very high frequency clocks.
 - Extrapolating results (400MHz) \rightarrow Minutiae extraction performed in 0'3 s.



Thanks for your assistance